12W Stereo Class-D Audio Power Amplifier

Features

- **Class-D Operation with High Efficiency.**
- **32-Step DC Volume Control With Hysteresis**
- **9W Per Channel Output Power into 8Ω Load at 12V, Class-D Output**
- **12W Per Channel Output into 6Ω Load at 12V, Class-D Output**
- **5V LDO Output for Powering APA4801 Headphone Driver**
- **Line Output for APA4801 Headphone Driver with DC Volume Control**
- **Low Current Consumption in Shutdown Mode (10μA, Typical)**
- **APA3002 will Auto-Recovery after Over-Current Protection**
- **Thermal and Over-Current Protections**
- **TQFN7x7-48 with Thermal Pad Package**
  TQFP7x7-48P with Thermal Pad Package
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APA3002 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo Class-D audio power amplifiers capable of producing 9W into 8Ω (12V) with less than 10% THD+N. The attenuator range of the volume control in the APA3002 is from 36dB (V_{VOLUME}=5V) to -40dB (V_{VOLUME}=0V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. The circuitries of both thermal and the over-current protections are integrated in the APA3002. It protects the chip from being destroyed by over temperature and over current failure.

To simplify the audio system design, the APA3002 combines a line output for external headphone driver with volume control and a 5V regulator for external headphone drive, where the speaker output can be switched off by the headphone jack's switch pin that connects to the APA3002's mode pin as shown in the application circuit.

Applications

- **LCD TV**
- **Active Speaker**

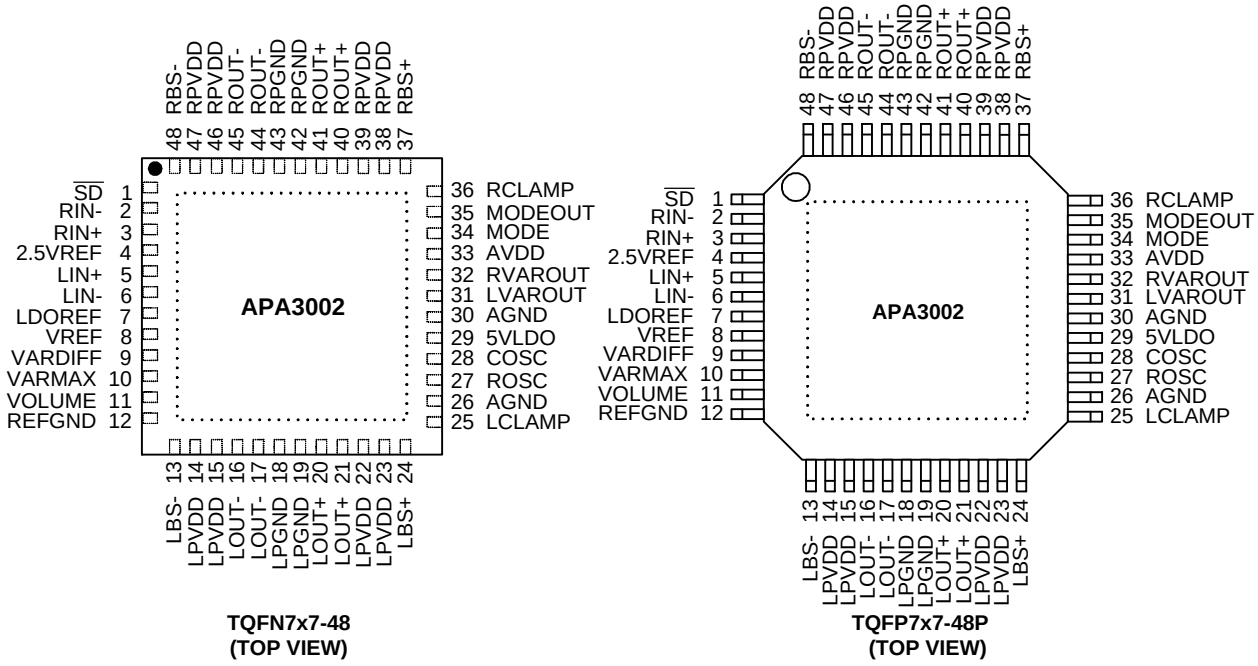
Ordering and Marking Information

APA3002 □□□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code QB: TQFN7x7-48 QCA: TQFP7x7-48P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR: Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3002 QB: 	XXXXX - Date Code
APA3002 QCA: 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configurations



TQFN7x7-48
(TOP VIEW)

TQFP7x7-48P
(TOP VIEW)

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (AVDD to AGND, LPVDD to LPGND, and RPVDD to RPGND)	-0.3 to 15	V
V_{MODE}, V_{VREF}, V_{VOLUME}, $V_{VARDIFF}$, V_{VARMAX}	Input Voltage (MODE to AGND, VREF, VOLUME, VARDIFF, and VARMAX to REFGND)	-0.3 to 5.5	V
$V_{\overline{SD}}$	Input Voltage ($\overline{SD}$ to AGND)	-0.3 to V_{DD}+0.3	
V_{RIN+}, V_{RIN-},V_{LIN+},V_{LIN-}	Input Voltage (RIN+, RIN-, LIN+, and LIN- to AGND)	-0.3 to 7	
	Input Voltage (RPGND and LPGND to AGND)	-0.3 to +0.3	
I_{5VLDO}	Output Current (5VLDO)	120	mA
I_{LDOREF}	Output Current (LDOREF)	20	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W
R_L	Class-D Power Amplifier Minimum Load Resistance	4	Ω

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2)	TQFN7x7-48 TQFP7x7-48P	21 25	°C/W

Note 2: Please refer to "Thermal Pad Consideration". The Thermal Pad on the bottom of the IC should be soldered directly to the PCB's Thermal Pad area connected to the ground plan by several thermal vias, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		8.5	14	V
	Volume Reference Voltage	VREF	3.0	5.5	V
	Volume Control Pin, Input Voltage	VOLUME, VARMAX, VARDIFF	-	5.5	V
V_{IH}	High-level Input Voltage	$\overline{SD}$	2	-	V
		MODE	3.5	-	V
V_{IL}	Low-level Input Voltage	$\overline{SD}$	-	0.8	V
		MODE	-	2	V
V_{OH}	High-level Output Voltage	MODEOUT sources 1mA	V_{5VLDO} -100m	-	V
V_{OL}	Low-level Output Voltage	MODEOUT sinks 1mA	-	+100m	V
f_{OSC}	Oscillator Frequency		225	275	kHz
T_A	Operating Free-Air Temperature		-40	85	℃
R_L	Class-D Power Amplifier Minimum Load Resistance		6	-	Ω

Electrical Characteristics

V_{DD} =12V, DGND=AGND=0V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Condition	APA3002			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		8.5	-	14	V
I_{DD}	V_{DD} Supply Current	Class-D mode, V_{MODE}=0V, $V_{\overline{SD}}$ =5V, no load	-	20	40	mA
		VAROUT mode, V_{MODE}=5V, $V_{\overline{SD}}$ =5V, no load	-	3	6	mA
I_{SD}	V_{DD} Shutdown Current	$V_{\overline{SD}}$ = 0V	-	10	100	µA
CLASS-D MODE, A_V=15.7dB (VOLTAGE GAIN=RATIO OF THE FILTERED OUTPUT VOLTAGE TO INPUT VOLTAGE)						
P_O	Output Power	THD+N = 1%, f_{in} = 1kHz, R_L = 6Ω	-	10	-	W
		THD+N = 1%, f_{in} = 1kHz, R_L = 8Ω	6	7.5	-	
		THD+N = 10%, f_{in} = 1kHz, R_L = 6Ω	-	12	-	
		THD+N = 10%, f_{in} = 1kHz, R_L = 8Ω	-	9	-	
THD+N	Total Harmonic Distortion Plus Noise	P_O= 5W, f_{in}= 1kHz, R_L = 8Ω	-	0.2	-	%
Crosstalk	Channel Separation	P_O= 5W, f_{in}=1kHz, C_B=1µF	-	90	-	dB
PSRR	Power Supply Rejection Ratio	R_L = 8Ω, f_{in} = 120Hz	-	85	-	dB

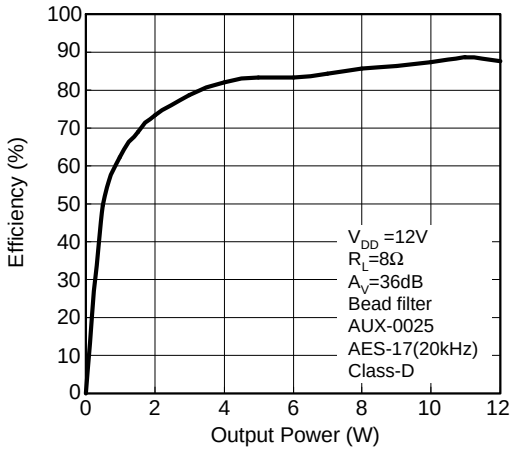
Electrical Characteristics (Cont.)

V_{DD} =12V, DGND=AGND=0V, T_A= 25°C (unless otherwise noted)

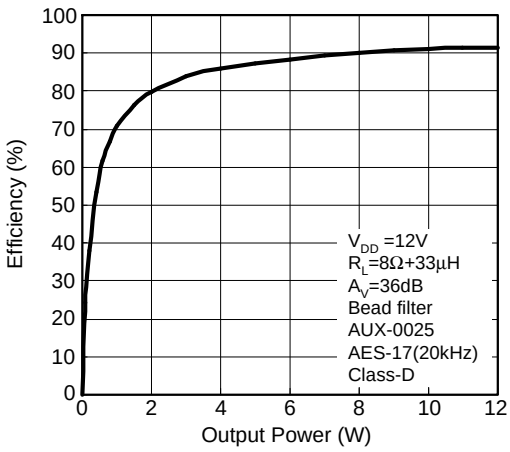
Symbol	Parameter	Test Condition		APA3002			Unit
				Min.	Typ.	Max.	
CLASS-D MODE, A_V=15.7dB (VOLTAGE GAIN=RATIO OF THE FILTERED OUTPUT VOLTAGE TO INPUT VOLTAGE) (CONT.)							
S/N		With A-Weighting Filter P_O = 5W, R_L = 8Ω		-	85	-	dB
V_{OS}	Output Offset Voltage	R_L = 8Ω		-	-	20	mV
V_n	Noise Output Voltage			-	250	-	μV (rms)
$R_{ds(on)}$	Power MOSFET Drain-Source On-State Resistance	I_O=1A	High side	-	300	-	mΩ
			Low side	-	250	-	
			Total	-	550	650	
VAROUT OUTPUT, A_V=10dB							
P_O	Output Power	THD+N = 1%, f_{in} = 1kHz, R_L = 32Ω		-	20	-	mW
		THD+N = 10%, f_{in} = 1kHz, R_L = 32Ω		-	25	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}= 1kHz, R_L = 32Ω, P_O = 14mW,		-	0.05	-	%
		V_O= 1V_{rms}, R_L=47kΩ, f_{in}=1kHz		-	0.005	-	
Crosstalk	Channel Separation	P_O=14mW, R_L = 32Ω, f_{in}=1kHz, C_B=1μF		-	63	-	dB
PSRR	Power Supply Rejection Ratio	C_B = 1μF, R_L = 32Ω, f_{in} =120Hz, V_{RR}=0.2V_{rms}		-	85	-	dB
V_{os}	Output Offset Voltage	R_L = 32Ω		-	-	20	mV
S/N		With A-Weighting Filter P_O= 20mW, R_L = 32Ω,		-	80	-	dB
V_n	Noise Output Voltage	C_B = 1μF		-	30	-	μV (rms)
LINEAR REGULATORS (LDO)							
V_{5VLDO}	5V LDO Regulator Output	I_{5VLDO} =0-100mA, $V_{\overline{SD}}$ =5V		4.5	5	5.5	V
$V_{2.5VREF}$	2.5V Reference Voltage	No load		0.45X V_{5VLDO}	0.50X V_{5VLDO}	0.55X V_{5VLDO}	V
PSRR	Power Supply Rejection Ratio	C_B = 1μF, f_{in}= 120Hz		-	73	-	dB

Typical Operating Characteristics

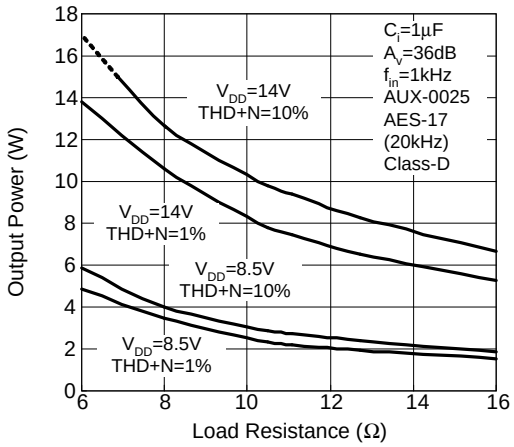
Efficiency vs. Output Power



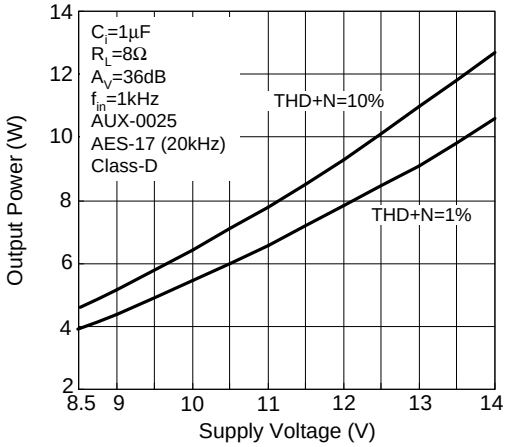
Efficiency vs. Output Power



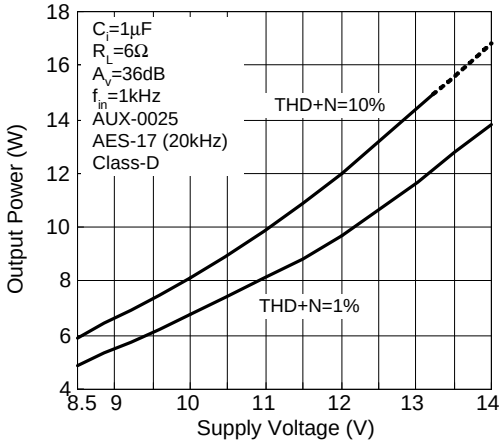
Output Power vs. Load Resistance



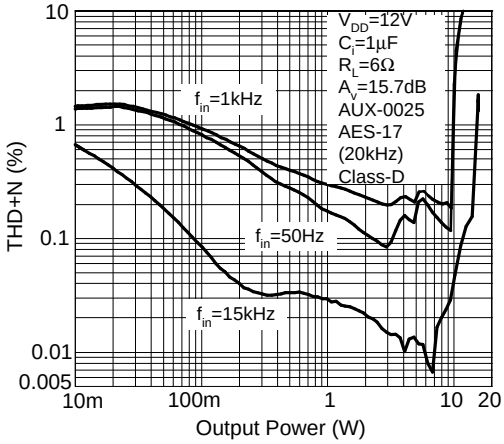
Output Power vs. Supply Voltage



Output Power vs. Supply Voltage

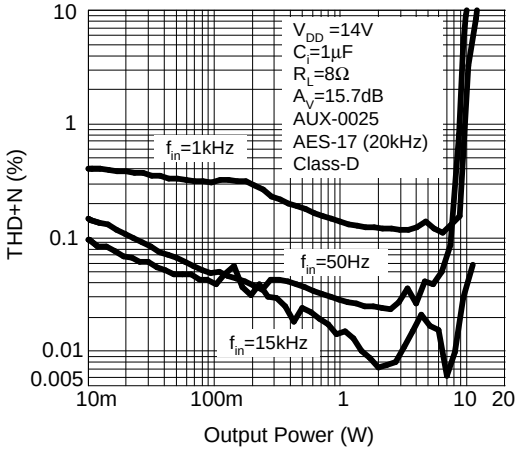


THD+N vs. Output Power

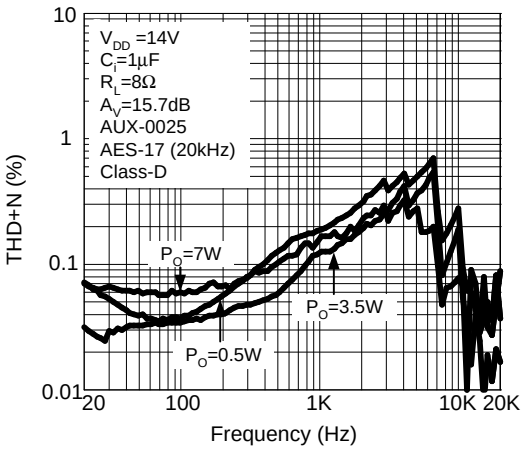


Typical Operating Characteristics (Cont.)

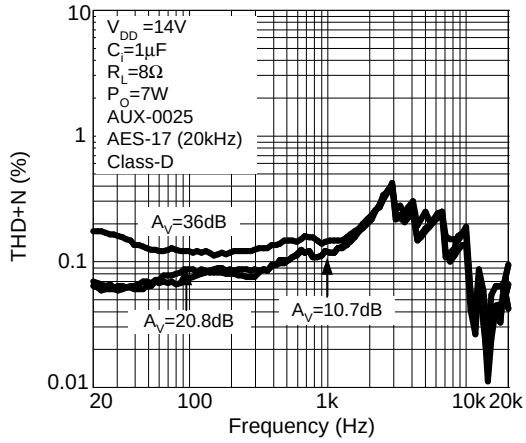
THD+N vs. Output Power



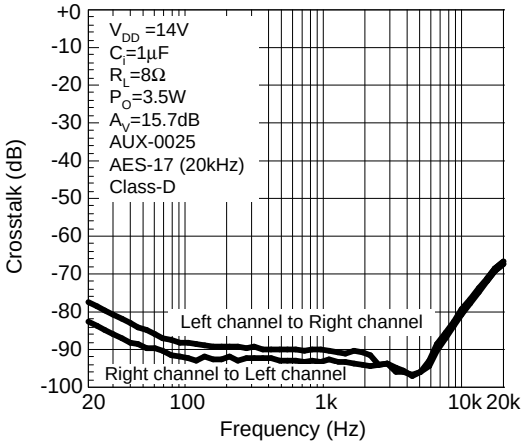
THD+N vs. Frequency



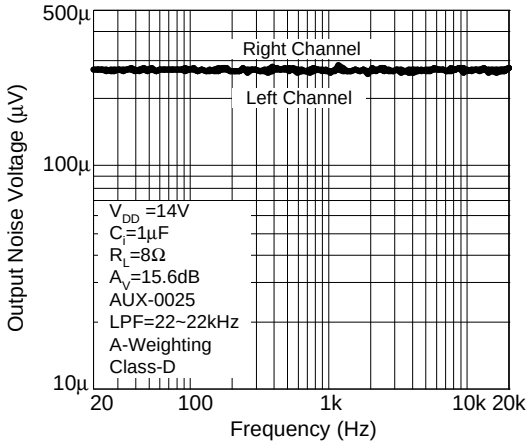
THD+N vs. Frequency



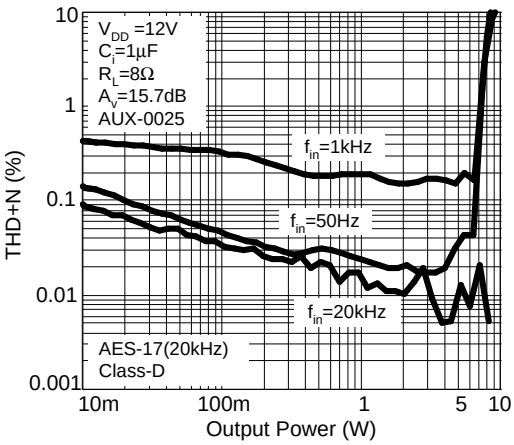
Crosstalk vs. Frequency



Noise vs. Frequency

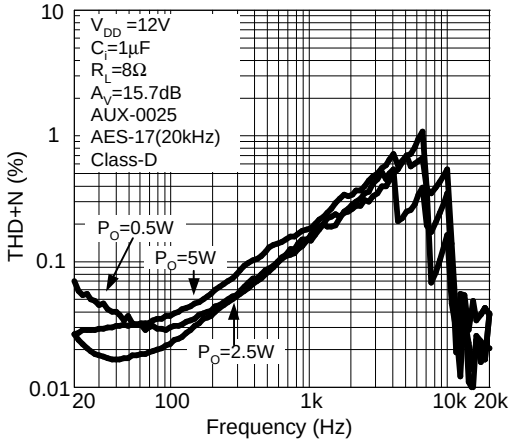


THD+N vs. Output Power

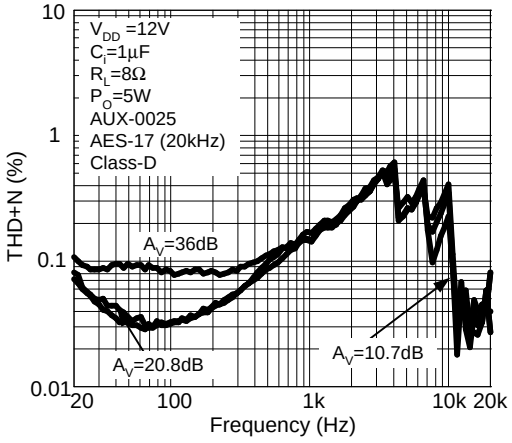


Typical Operating Characteristics (Cont.)

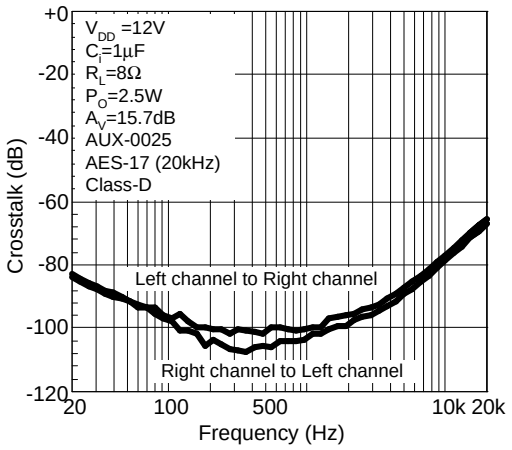
THD+N vs. Frequency



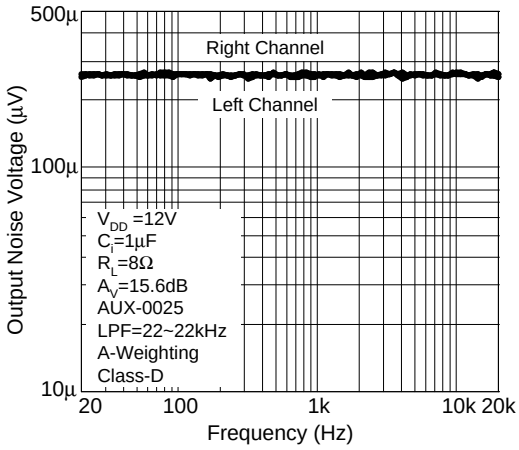
THD+N vs. Frequency



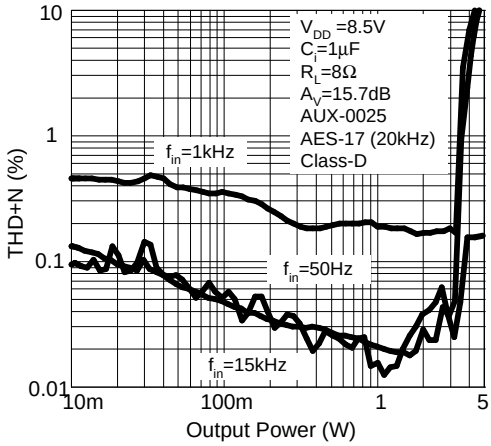
Crosstalk vs. Frequency



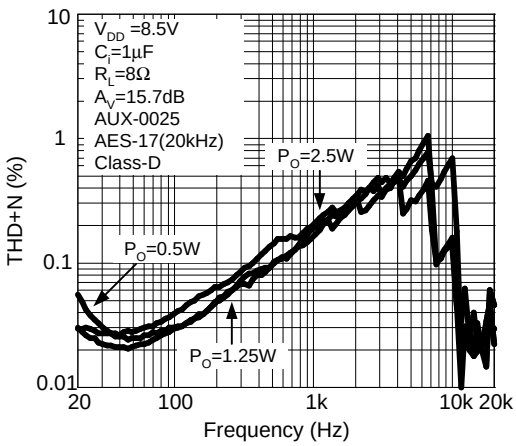
Noise vs. Frequency



THD+N vs. Output Power

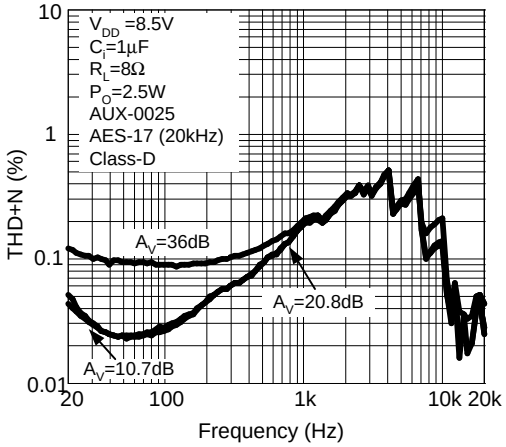


THD+N vs. Frequency

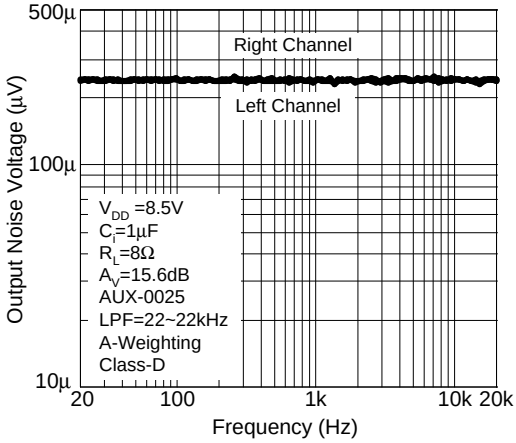


Typical Operating Characteristics (Cont.)

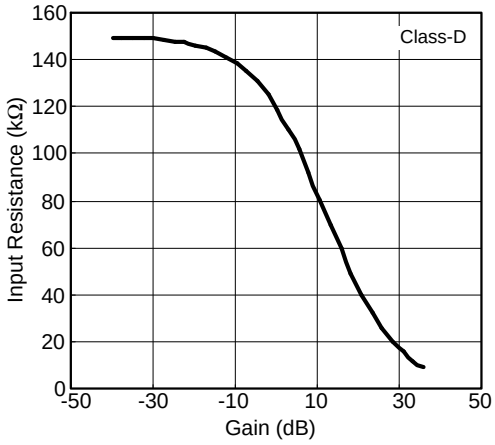
THD+N vs. Frequency



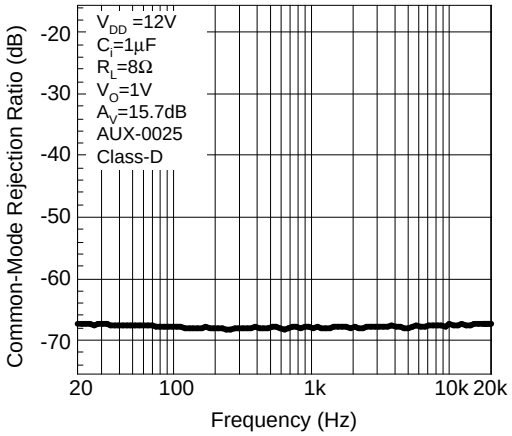
Noise vs. Frequency



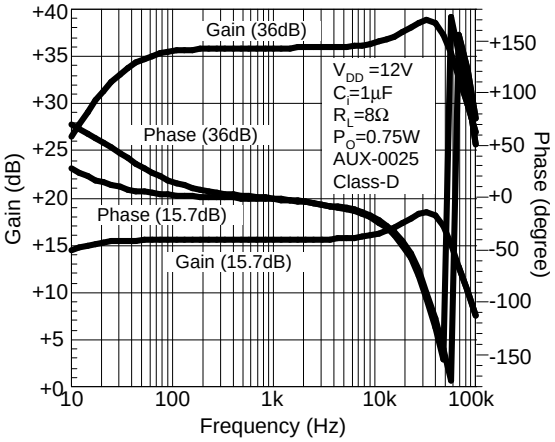
Input Resistance vs. Gain



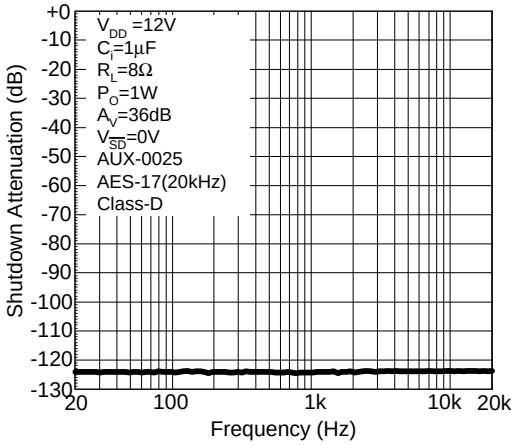
CMRR vs. Frequency



Frequency Response

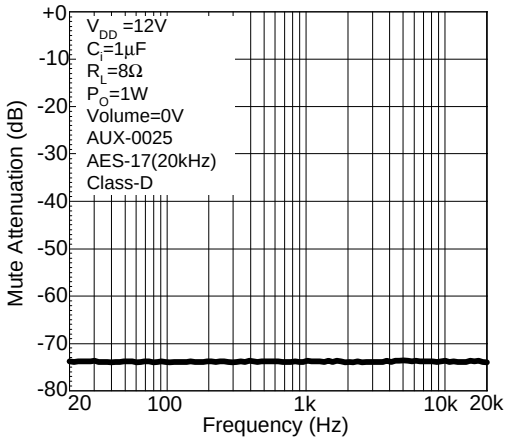


Shutdown Attenuation vs. Frequency

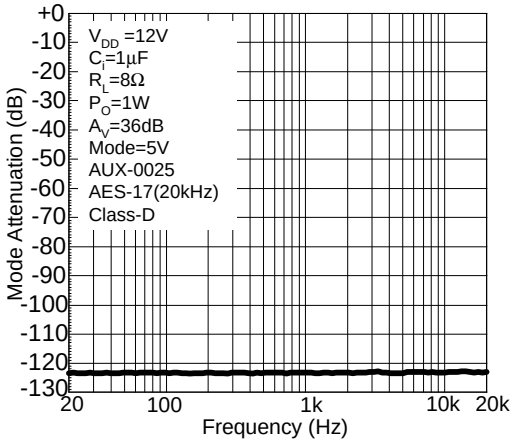


Typical Operating Characteristics (Cont.)

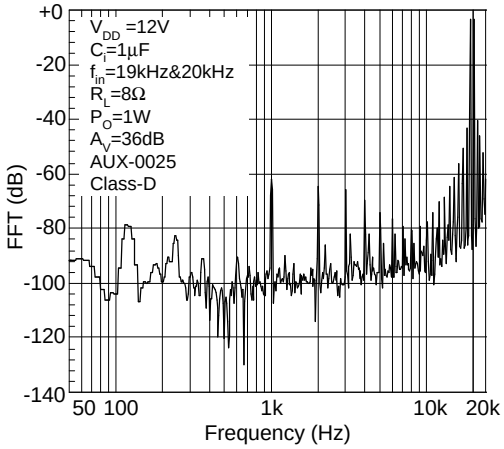
Mute Attenuation vs. Frequency



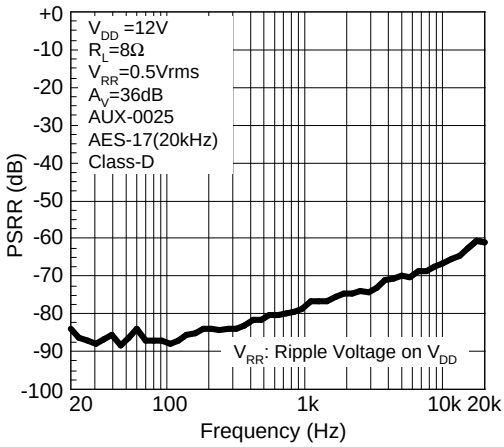
Mode Attenuation vs. Frequency



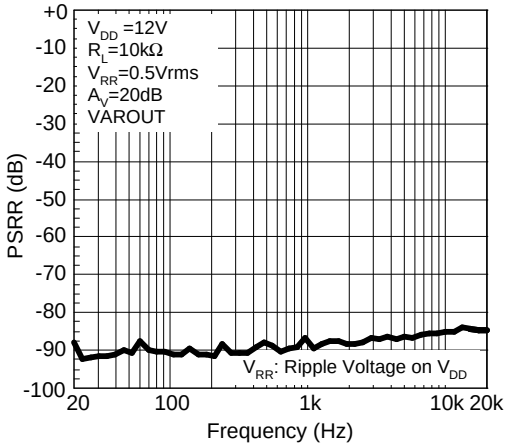
Inter-modulation Performance



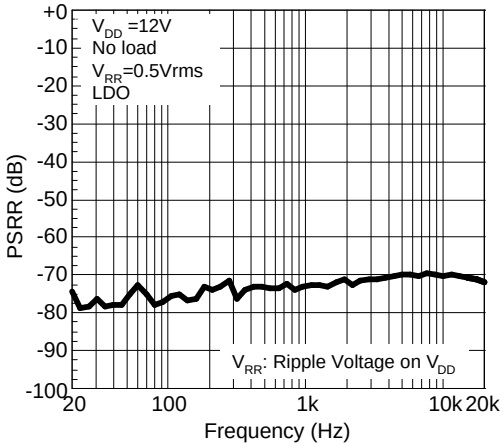
PSRR vs. Frequency



PSRR vs. Frequency

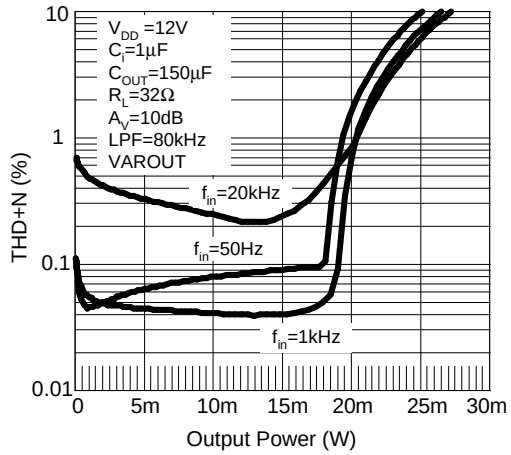


PSRR vs. Frequency

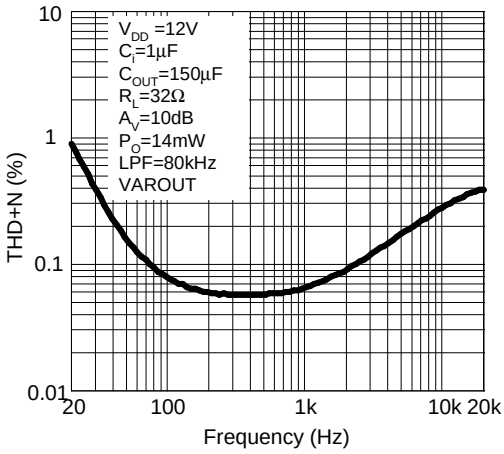


Typical Operating Characteristics (Cont.)

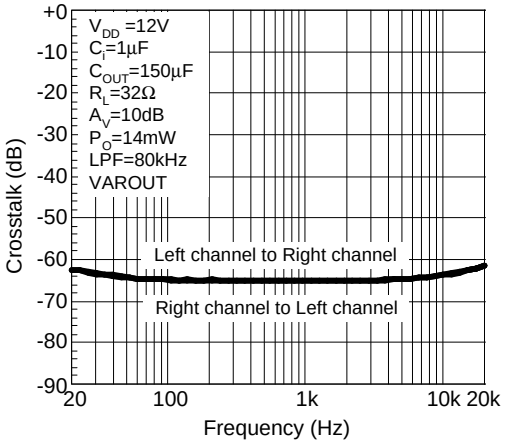
THD+N vs. Output Power



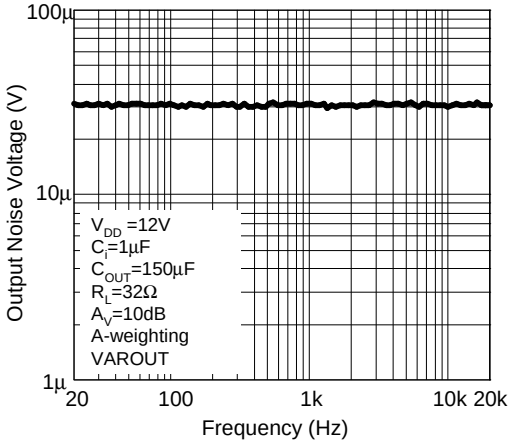
THD+N vs. Frequency



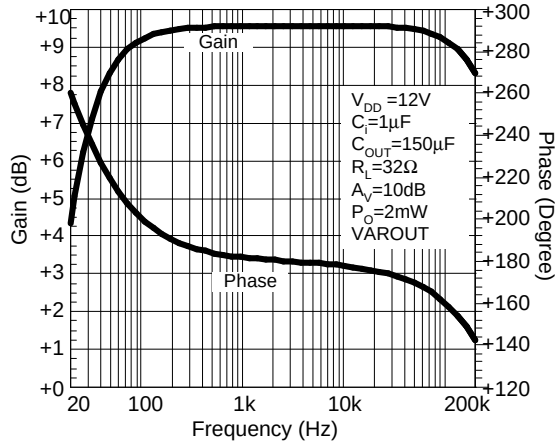
Crosstalk vs. Frequency



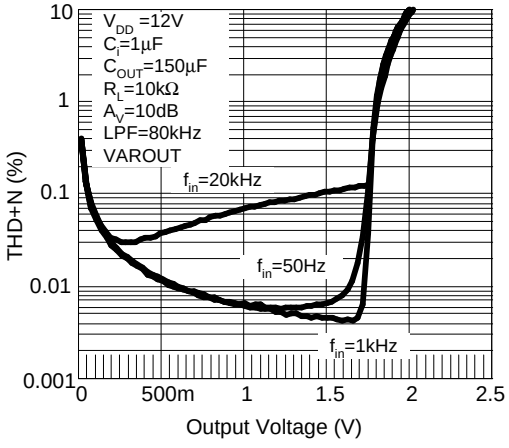
Noise vs. Frequency



Frequency Response

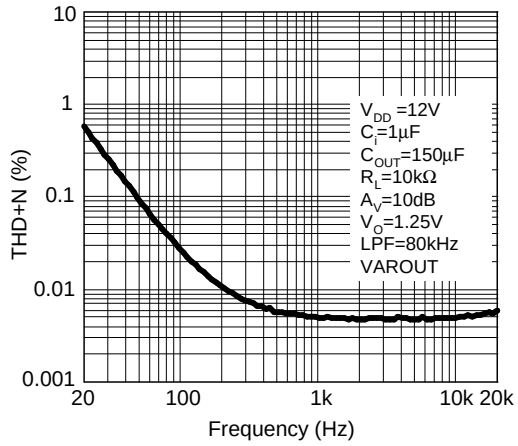


THD+N vs. Output Voltage

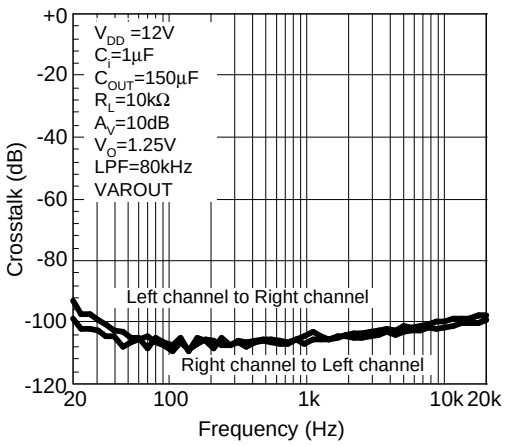


Typical Operating Characteristics (Cont.)

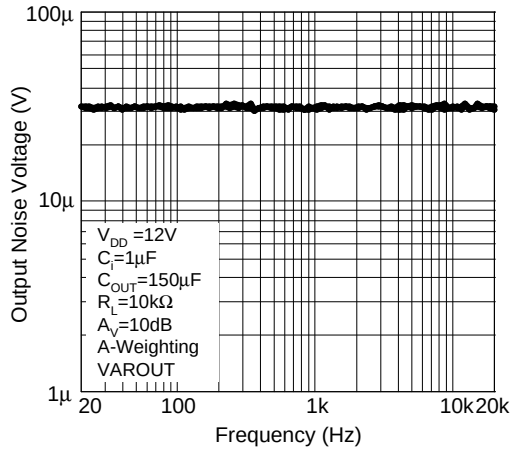
THD+N vs. Frequency



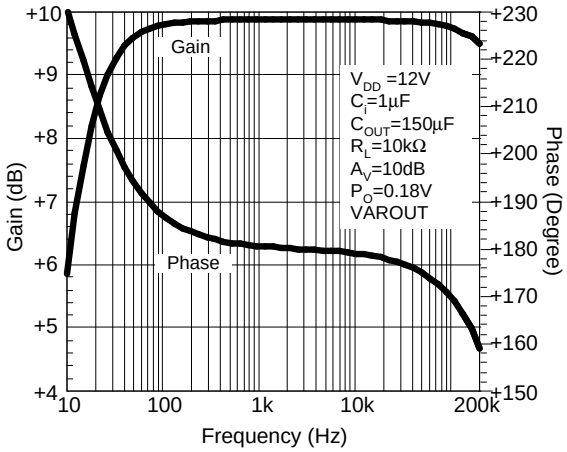
Crosstalk vs. Frequency



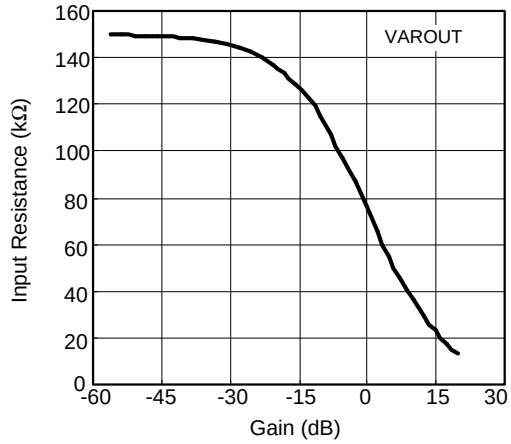
Noise vs. Frequency



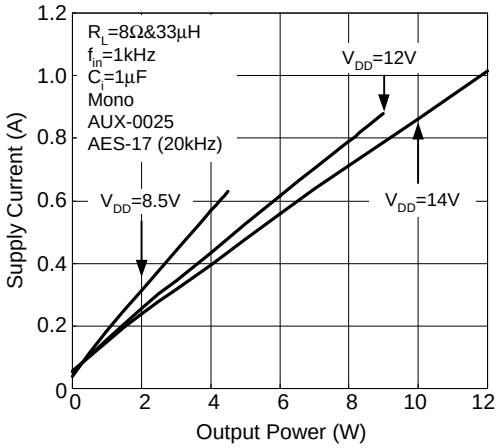
Frequency Response



Input Resistance vs. Gain

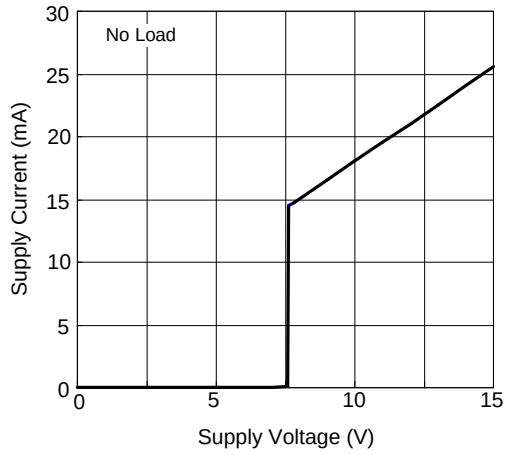


Supply Current vs. Output Power



Typical Operating Characteristics (Cont.)

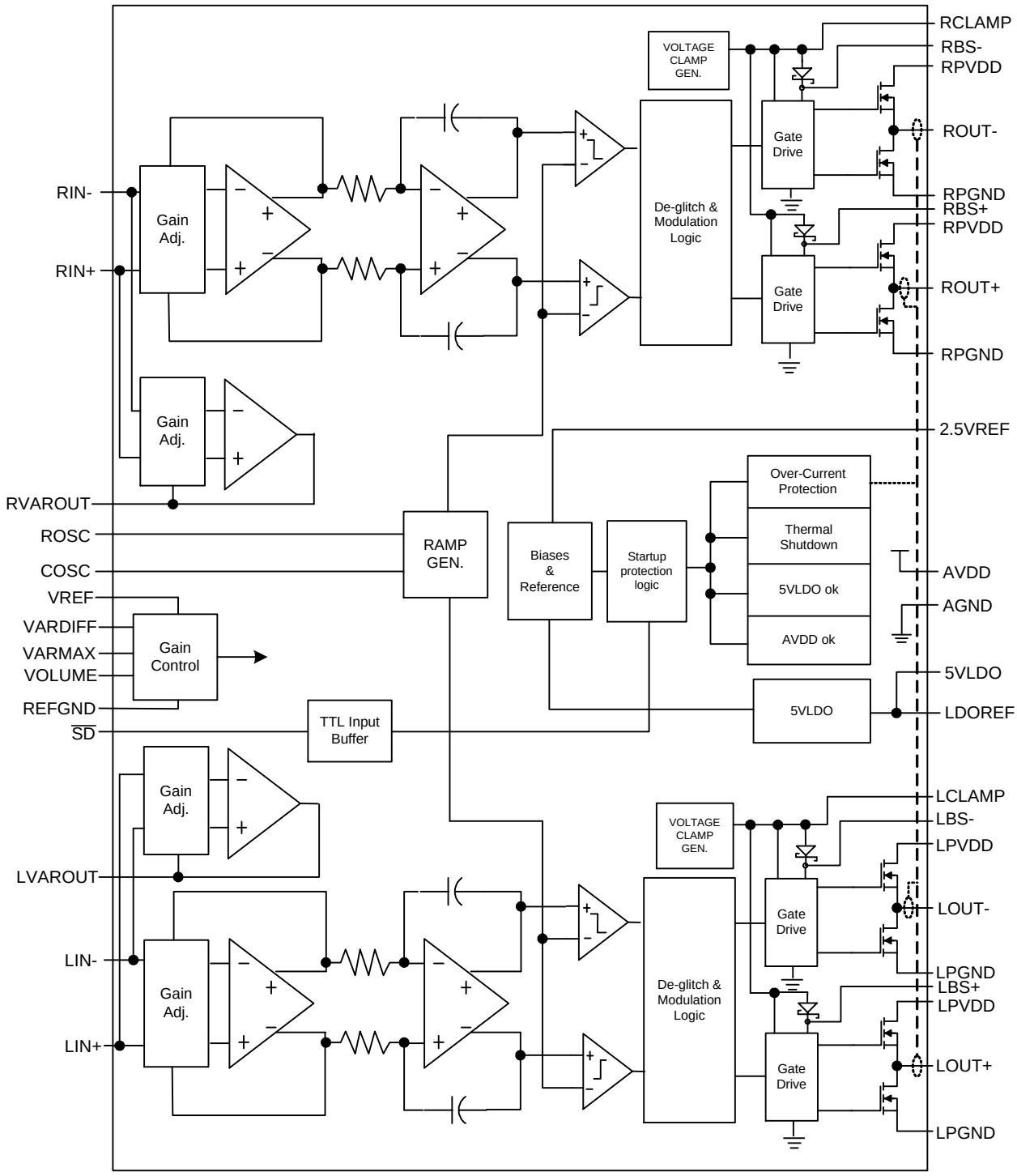
Supply Current vs. Supply Voltage



Pin Description

PIN		I/O	FUNCTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown mode control signal input. Pulling the voltage on $\overline{SD}$ below 0.8V makes the IC enter low-power shutdown mode with 10μA (typical) I_{DD}.
2	RIN-	I	Right channel negative input.
3	RIN+	I	Right channel positive input.
4	2.5VREF	O	2.5V reference for analog circuits.
5	LIN+	I	Left channel positive input.
6	LIN-	I	Left channel negative input.
7	LDOREF	O	5V reference output (5V LDO), connect it to VREF pin.
8	VREF	I	Gain control section's reference voltage input.
9	VARDIFF	I	Input pin to set the difference in gain between the VAROUT and Class-D outputs by using the DC voltage. Connect this pin to the ground or LDOREF when the VAROUT is not used.
10	VARMAX	I	Input pin to set the maximum gain of VAROUT by using the DC voltage. Connect this pin to ground or LDOREF directly when the VAROUT is not used.
11	VOLUME	1	Input pin to set the gain of VAROUT and Class-D outputs by using the DC voltage.
12	REFGND	-	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
13	LBS-	I/O	Left channel bootstrap power input for negative high-side MOSFET.
14,15,22,23	LPVDD	-	Power supply for left channel H-bridge.
16,17	LOUT-	O	Class-D left channel negative output.
18,19	LPGND	-	Power ground for left channel H-bridge.
20,21	LOUT+	O	Class-D left channel positive output.
24	LBS+	I/O	Left channel bootstrap power input for positive high-side MOSFET.
25	LCLAMP	-	Left channel internal voltage supply output for bootstrap capacitor.
26,30	AGND	-	Analog ground.
27	ROSC	I/O	Voltage of ROSC pin equal $0.125V_{DD}$, current setting resistor for internal ramp generator.
28	COSC	I/O	Charge/Discharge capacitor for generating triangle wave.
29	5VLDO	O	Internal 5V regulator output for external headphone driver used.
31	LVAROUT	O	Left channel variable audio output, for external headphone driver.
32	RVAROUT	O	Right channel variable audio output, for external headphone driver.
33	AVDD	-	Analog power supply (8.5 to 14V).
34	MODE	I	Control pin for amplifier operation. A logic high places the amplifier in variable output mode, and the Class-D output will disable; a logic low places the amplifier in variable output mode (line-level output for external amplifier) and stereo Class-D outputs.
35	MODEOUT	O	Inverse output of MODE pin, this pin can control the external headphone driver's (APA4801) mute pin for changing operation from speaker operation to headphone operation. Leave this pin unconnected when the external headphone driver is not in using.
36	RCLAMP	-	Right channel internal voltage supply output for bootstrap capacitor.
37	RBS+	I/O	Right channel bootstrap voltage input for positive high-side MOSFET.
38,39,46,47	RPVDD	-	Power supply for right channel H-bridge.
40,41	ROUT+	O	Class-D right channel positive output.
42,43	RPGND	-	Power ground for right channel H-bridge.
44,45	ROUT-	O	Class-D right channel negative output.
48	RBS-	I/O	Right channel bootstrap voltage input for negative high-side MOSFET.

Block Diagram



Operating Mode Selection Table

MODE	$\overline{SD}$	Operating mode
H	L	Shutdown mode
L	H	Class-D operation
H	H	Class-D disable, VAROUT output.

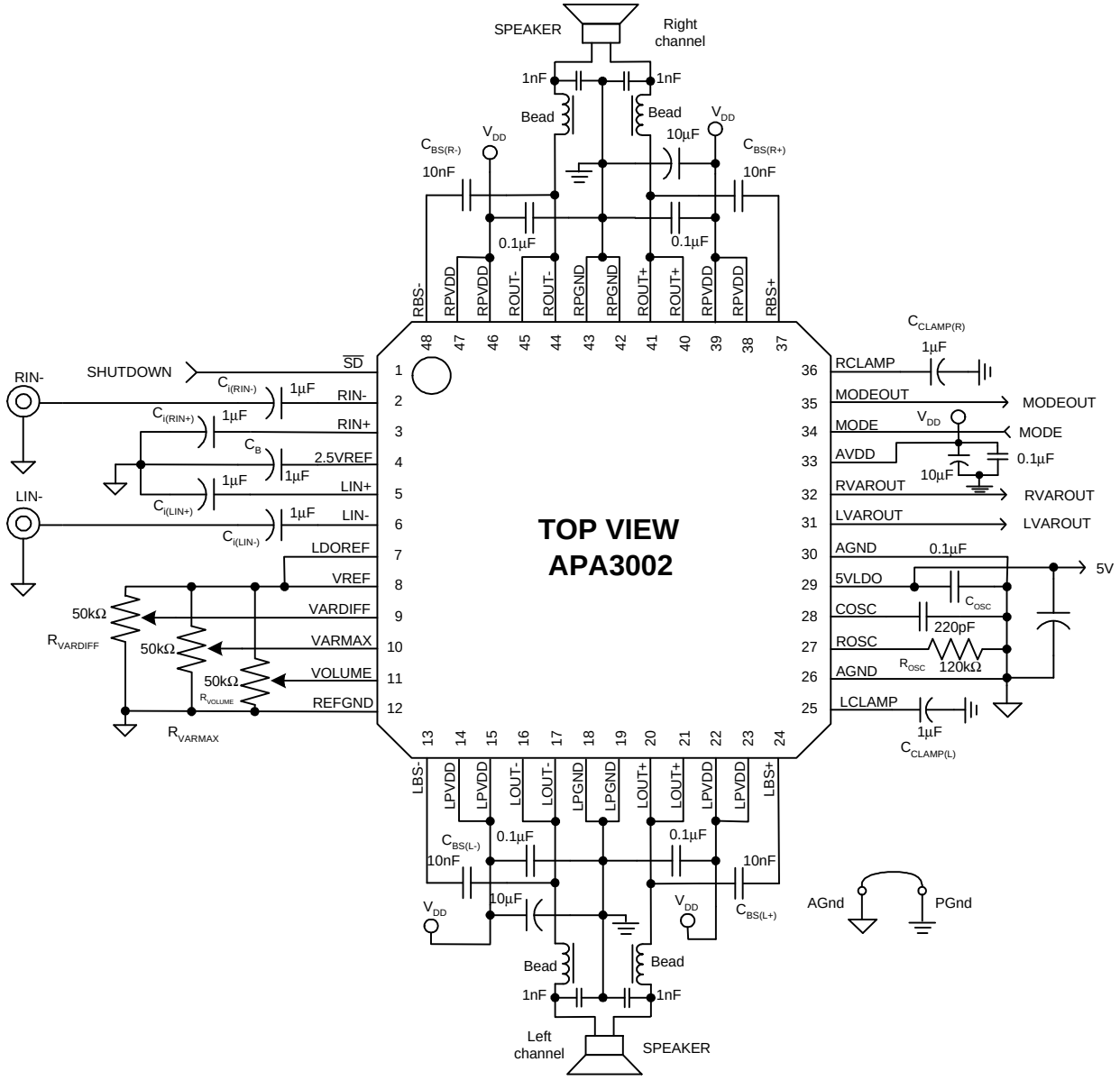
Class-D DC Volume Control Table

GAIN	Voltage range (% of V_{VREF})	
	Increasing V_{VOLUME}	Decreasing V_{VOLMUE}
(dB)	(%)	(%)
-75	0 -4.5	0 -2.9
-40	4.5 -6.7	2.9 -5.1
-37.5	6.7 -8.9	5.1 -7.2
-35	8.9 -11.1	7.2 -9.4
-32.4	11.1 -13.3	9.4 -11.6
-29.9	13.3 -15.5	11.6 -13.8
-27.4	15.5 -17.7	13.8 -16.0
-24.8	17.7 -19.9	16.0 -18.2
-22.3	19.9 -22.1	18.2 -20.4
-19.8	22.1 -24.3	20.4 -22.6
-17.2	24.3 -26.5	22.6 -24.8
-14.7	26.5 -28.7	24.8 -27.0
-12.2	28.7 -30.9	27.0 -29.1
-9.6	30.9 -33.1	29.1 -31.3
-7.1	33.1 -35.3	31.3 -33.5
-4.6	35.3 -37.5	33.5 -35.7
-2	37.5 -39.7	35.7 -37.9
0.5	39.7 -41.9	37.9 -40.1
3.1	41.9 -44.1	40.1 -42.3
5.6	44.1 -46.4	42.3 -44.5
8.1	46.4 -48.6	44.5 -46.7
10.7	48.6 -50.8	46.7 -48.9
13.2	50.8 -53	48.9 -51.0
15.7	53 -55.2	51.0 -53.2
18.3	55.2 -57.4	53.2 -55.4
20.8	57.4 -59.6	55.4 -57.6
23.3	59.6 -61.8	57.6 -59.8
25.9	61.8 -64	59.8 -62.0
28.4	64 -66.2	62.0 -64.2
30.9	66.2 -68.4	64.2 -66.4
33.5	68.4 -70.6	66.4 -68.4
36	>70.6	>68.6

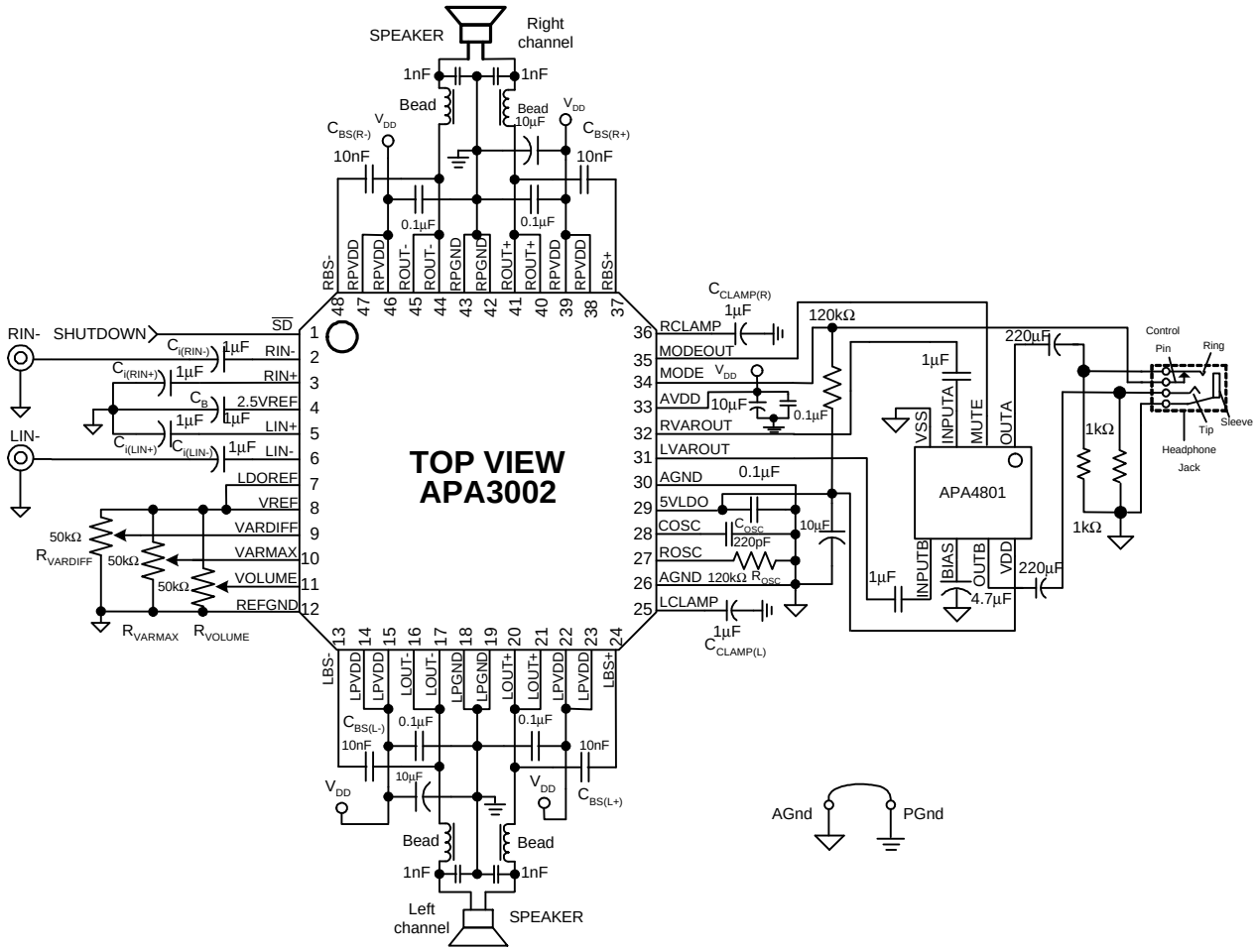
VAROUT VOLUME Control Table

GAIN	Voltage range (% of V_{VREF})	
	Increasing V_{VOLUME}	Decreasing V_{VOLMUE}
(dB)	(%)	(%)
-66	0 -4.5	0 -2.9
-56	4.5 -6.7	2.9 -5.1
-53.5	6.7 -8.9	5.1 -7.2
-50.9	8.9 -11.1	7.2 -9.4
-48.4	11.1 -13.3	9.4 -11.6
-45.9	13.3 -15.5	11.6 -13.8
-43.3	15.5 -17.7	13.8 -16.0
-40.8	17.7 -19.9	16.0 -18.2
-38.3	19.9 -22.1	18.2 -20.4
-35.7	22.1 -24.3	20.4 -22.6
-33.2	24.3 -26.5	22.6 -24.8
-30.7	26.5 -28.7	24.8 -27.0
-28.1	28.7 -30.9	27.0 -29.1
-25.6	30.9 -33.1	29.1 -31.3
-23.1	33.1 -35.3	31.3 -33.5
-20.5	35.3 -37.5	33.5 -35.7
-18.0	37.5 -39.7	35.7 -37.9
-15.5	39.7 -41.9	37.9 -40.1
-13.0	41.9 -44.1	40.1 -42.3
-10.4	44.1 -46.4	42.3 -44.5
-7.9	46.4 -48.6	44.5 -46.7
-5.3	48.6 -50.8	46.7 -48.9
-2.8	50.8 -53	48.9 -51.0
-0.3	53 -55.2	51.0 -53.2
2.3	55.2 -57.4	53.2 -55.4
4.8	57.4 -59.6	55.4 -57.6
7.3	59.6 -61.8	57.6 -59.8
9.9	61.8 -64	59.8 -62.0
12.4	64 -66.2	62.0 -64.2
14.9	66.2 -68.4	64.2 -66.4
17.5	68.4 -70.6	66.4 -68.4
20.0	>70.6	>68.6

Typical Application Circuits



Typical Application Circuits (Cont.)



Application Information

Class-D Operation

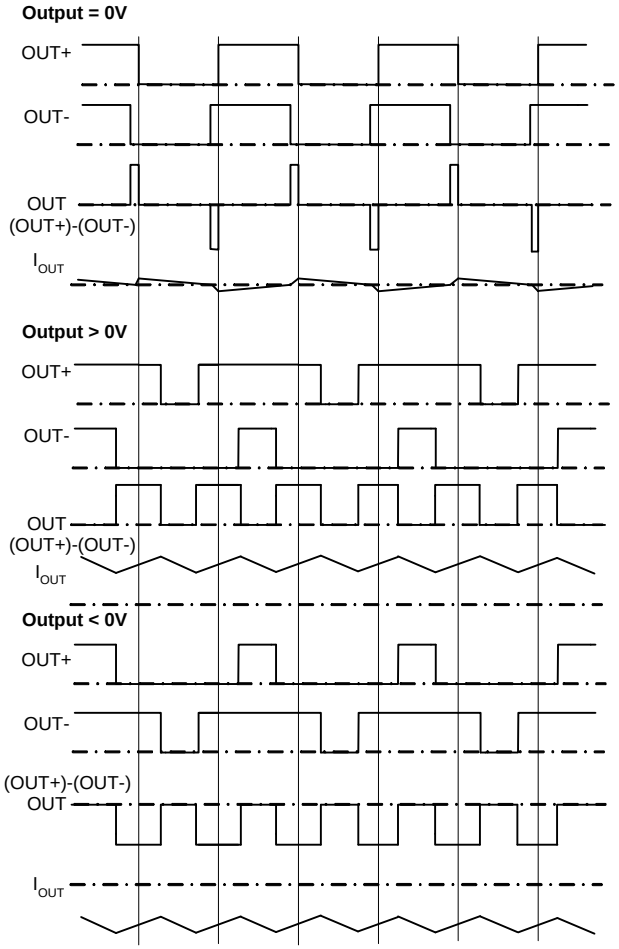


Figure1. APA3002 Output Waveform (Voltage & Current)

The APA3002 modulation scheme is shown in Figure 1, the outputs OUT+ and OUT- are in phase with each other when no input signals. When output > 0V, the duty cycle of OUT+ is greater than 50% and OUT- is less than 50%; on the contrary, when output <0V, the duty cycle of OUT+ is less than 50% and OUT- is greater than 50%. This method reduces the switching current across the load and reduces the I^2R loss in the load that improves the amplifier's efficiency.

This modulation scheme has very short pulses across the load. This makes the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Adding the LC filter can increase the efficiency by filter the ripple current.

Square Wave Into the Speaker

To apply the square wave into the speaker may cause the voice coil of speaker jumps out the air gap and defaces the voice coil. However, this depends on if the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 250kHz switching frequency, this is not an issue for the speaker because the frequency is beyond the audio band, and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor (R_i)

In order to achieve the 32 steps gain setting, the R_i varies the input resistance network (R_i & R_f) of amplifier. The input resistor's range from the smallest to the maximum is about 15 times, therefore, the input high-pass filter's low cutoff frequency will change 15 times from low to high. The cutoff frequency can be calculated by equation 1.

Input Capacitor (C_i)

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i form a high-pass filter with the corner frequency is determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example, where R_i is 10kΩ and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.40μF, so a value in the range of 0.47μF to 1.0μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom,

Application Information (Cont.)

Input Capacitor (C_i) (Cont.)

especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' inputs is held at 2.5VREF. Please note that it is important to confirm the capacitor polarity in the application.

C_{osc} & R_{osc}

The Class-D amplifier's switching frequency is determined by the component that connected to ROSC (pin) and COSC (pin). The frequency can be calculated by the following equation:

$$f_{osc} = \frac{6.6}{R_{osc}C_{osc}} \quad (3)$$

BS+ &BS- Capacitor (C_{BS})

Since the Full-bridge output stages are only using the N-channel power MOSFET, the high-side MOSFET's driver needs bootstrap circuit to turn on the high side power MOSFET correctly. A 10nF/35V ceramic capacitor is recommended.

The bootstrap capacitors are like floating power supply for high side N-channel power MOSFET gate driver. The bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side N-channel power MOSFET turn-on at high side switching cycle. At the high-side turn-on cycle, the voltage of bootstrap capacitors will decrease through the leakage path. The bootstrap voltage can decrease below the minimum Vgs that required to keep the high-side N-channel power MOSFET turn-on, if driving into heavy clipping with a less than 50Hz sine wave. When this occurs, the output power MOSFET becomes source-follower and the output drops from V_{DD} to approximately Vclamp.

Driving a square wave at low frequencies is not a design consideration for majority application, so the 10nf bootstrap capacitor is recommended. If the low frequency is a concern, please increase the bootstrap capacitor value to hold the gate voltage for a longer period and the voltage drop will not occur.

CLAMP Capacitor (C_{CLAMP})

These capacitors are regulated the clamp voltage of N-channel power MOSFET's gate voltage, ensuring the maximum gate-to-source voltage of the MOSFET not to exceed. 1µF/25V capacitors are recommended.

Power Supply Decoupling (C_s)

The APA3002 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically is 0.1µF which is placed as close as possible to the device VDD lead to achieve the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Ferrite Bead Selection

If the traces from the APA3002 to speaker are short, the ferrite bead filters can reduce the high frequency radiated to meet the FCC & CE's requirements.

A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output LC Filter

If the traces from the APA3002 to speaker are short, it doesn't require output filter for FCC & CE standard. Figure 2 is an example for adding the LC filter, it's recommended for the situation that the trace from amplifier to speaker is too long, and needed to eliminate the radiated emission or EMI.

Application Information (Cont.)

Output LC Filter (Cont.)

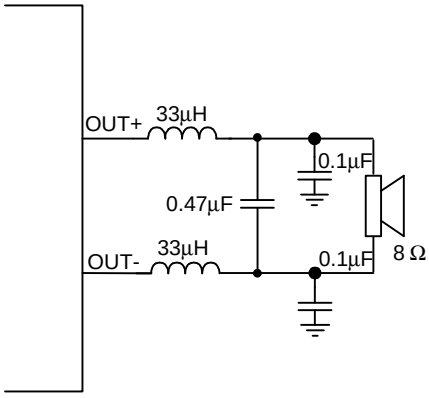


Figure 2. LC Output Filter

DC Volume

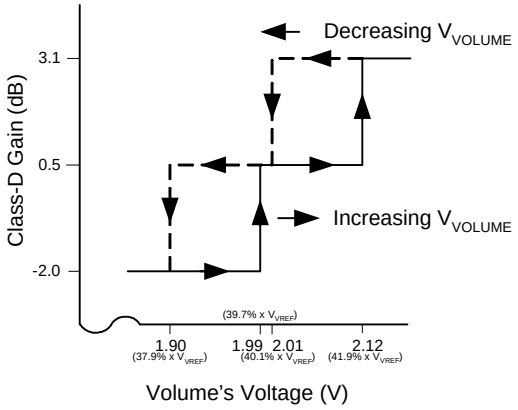


Figure 3. DC Volume Control Operation (V_{VREF}=5V)

The Class-D's gain is determined by the voltage of VOLUME control pin. "Class-D DC Volume Control Table" lists the gain in Class-D that is determined by the VOLUME pin's voltage (V_{VOLUME}) in reference to the VREF's voltage (V_{VREF}). The maximum voltage of VOLUME should not exceed the VREF's voltage.

If the resistor divider fixed the Class-D's gain is used, and then the resistor divider values to center the voltage between the two percentage points of the table's column "Increasing V_{VOLUME}" need to be calculated, see figure 3. The resistor can be connected between VREF and REFGND, and then VREF and LDOREF are connected together.

If a DAC controls the Class-D gain is used, VREF and REFGND should be connected to the reference voltage for the DAC and the GND terminal of the DAC respectively. For the DAC application, LDOREF would be left unconnected. The reference voltage of the DAC provides the reference to the internal gain circuitry through the VREF input and any fluctuations in the DAC output voltage will not affect the Class-D gain.

The percentages in the "Increasing V_{VOLUME}" of table should be used for setting the voltages of the DAC when the voltage on the VOLUME pin is increased. The percentages in the " decreasing V_{VOLUME}" of the table should be used for the DAC voltages when decreasing the voltage on the VOLUME pin. Two lookup tables should be used in software to control the gain based on an increase or decrease in the desired system volume.

If using an analog potentiometer to control the gain, it should be connected between VREF and REFGND. VREF can be connected to LDODREF or an external voltage source, if desired. The table of "Increasing V_{VOLUME}" and "Decreasing V_{VOLUME}" in "Class-D DC Volume Control Table" should be used to determine the point at which gain changes depending on the direction that the potentiometer is turned. If the voltage on the center tap of the potentiometer is increasing, the table "Increasing V_{VOLUME}" at "Class-D DC Volume Control Table" should be referenced to determine the trip points. If the voltage is decreasing, the trip points in the "Decreasing V_{VOLUME}" should be referenced.

The trip point, where the gain actually changes, is various depending on whether the voltage on the VOLUME pin is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 3. The graph focuses on three gain steps with the trip points defined in the table "Increasing V_{VOLUME}" and "Decreasing V_{VOLUME}" of "Class-D DC Volume Control Table" for Class-D gain. The dotted lines represent the hysteresis about each gain step.

Application Information (Cont.)

DC Volume

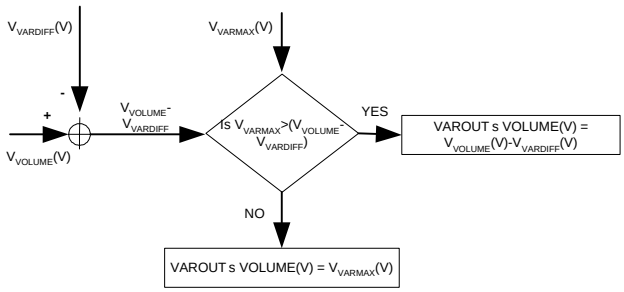


Figure 4. VAROUT Volume Control Flow

Three pins, VOLUME, VARMAX, and VARDIFF, determine the VAROUT's gain. The figure 4 shows the VAROUT volume control flow. All the values are DC voltage, and the V_{AROUT} channel gain can be determined by consulting the table "VAROUT VOLUME Control Table".

VARMAX

The VARMAX limits the maximum gain of VAROUT channels to avoid the un-comfortable listening of headphone.

VARDIFF

To avoid the uncomfortable listening when headphone is plugging, the VARDIFF sets the different gain between the Class-D and VAROUT channels. At initial ($V_{VARDIFF}$=0V), the difference gain between the Class-D and VAROUT is 16dB. When voltage of VARDIFF is increasing, the VAROUT's gain decreases.

MODE Operation

The mode controls the output mode of the APA3002, a logic "HIGH" will disable the Class-D outputs; a logic "LOW" will enable the Class-D outputs. This pin can connect to the switch on the headphone jack to disable the Class-D outputs when headphone plug is inserted. The "Typical Application Circuit " shows an example for this application.

MODE_OUT Operation

The MODE_OUT is the inverting output of MODE, and it controls the external headphone amplifier's $\overline{SD}$ pin (like the APA4801) for switching the Speaker mode or headphone.

LDO Operation

The 5VLOD terminal is the output of an internal-generated 5V power supply that is used for oscillator, preamplifier and DC volume control circuitry. The regulator can be powered the external headphone amplifier like the APA4801, or other circuitry, up to the current limit of 5VLDO pin (on specification table). With 10µF & 0.1µF capacitors connected to the terminal are recommended if powered by the APA4801; however, if there is no other larger loading, 1µF and 0.1µF are sufficient enough.

Shutdown Function

In order to reduce power consumption when not in use, the APA3002 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for the APA3002. The trigger point between a logic high and logic low level is typically 1.2V. It will be the best to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{SD}$ pin to low level, the amplifier enters a low-consumption-current state, I_{DD} for the APA3002 is in shutdown mode. Under normal operating, APA3002's $\overline{SD}$ pin should pull to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state change.

Thermal Pad Consideration

The thermal pad must be connected to the ground. The package with thermal pad of the APA3002 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA3002 will go into thermal shutdown. The thermal pad on the bottom of the APA3002 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 10 to 16 vias of 15 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should

Application Information (Cont.)

Thermal Pad Consideration (Cont.)

be as large as practical. If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA3002 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown. See TQFP7x7-48 thermal pad layout recommendation.

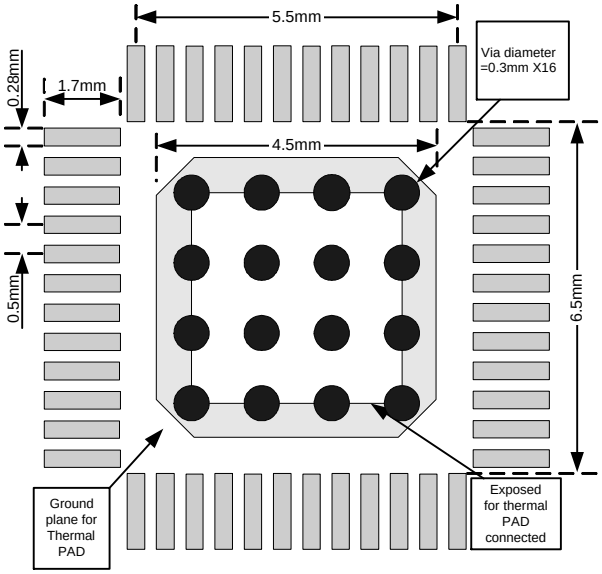
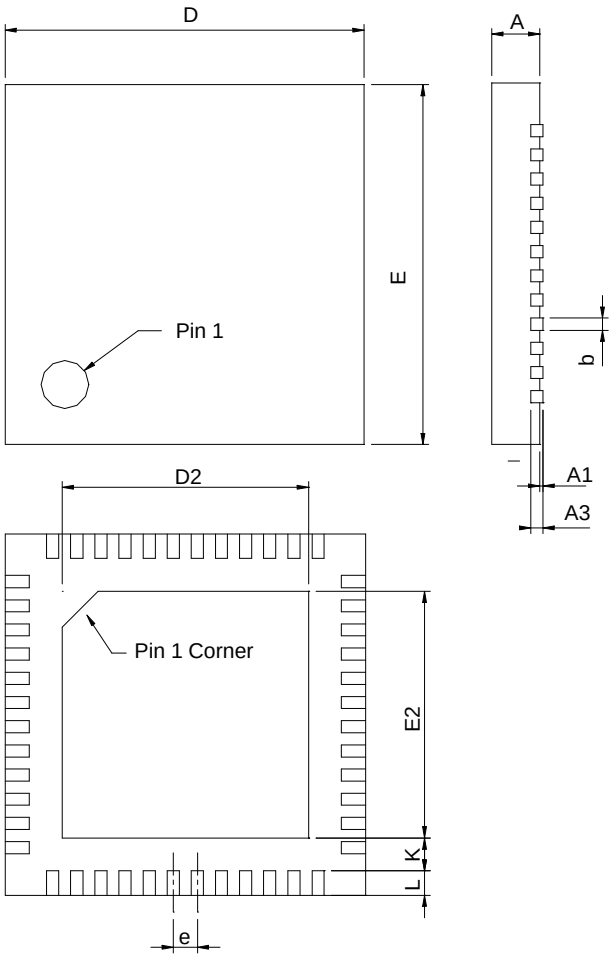


Figure 5. TQFP7x7-48 thermal pad layout recommendation

Package Information

TQFN7x7-48

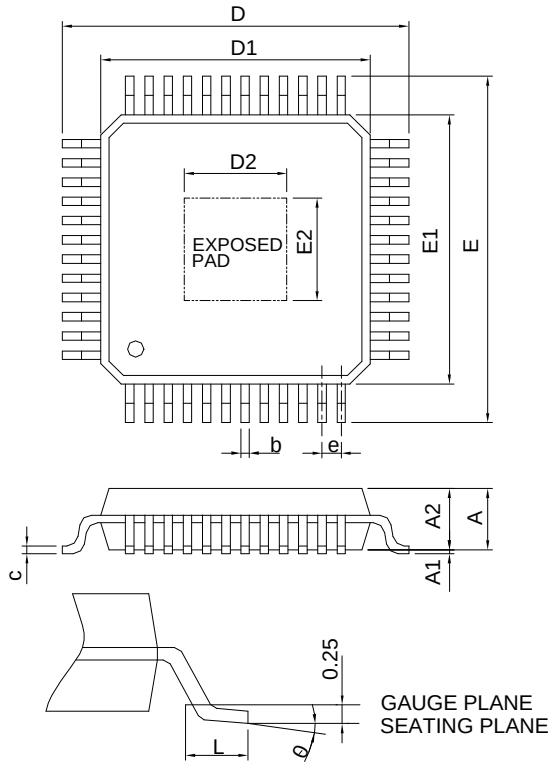


SYMBOL	TQFN7x7-48			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.90	7.10	0.272	0.280
D2	5.50	5.80	0.217	0.228
E	6.90	7.10	0.272	0.280
E2	5.50	5.80	0.217	0.228
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WKKD-4.

Package Information

TQFP7x7-48P

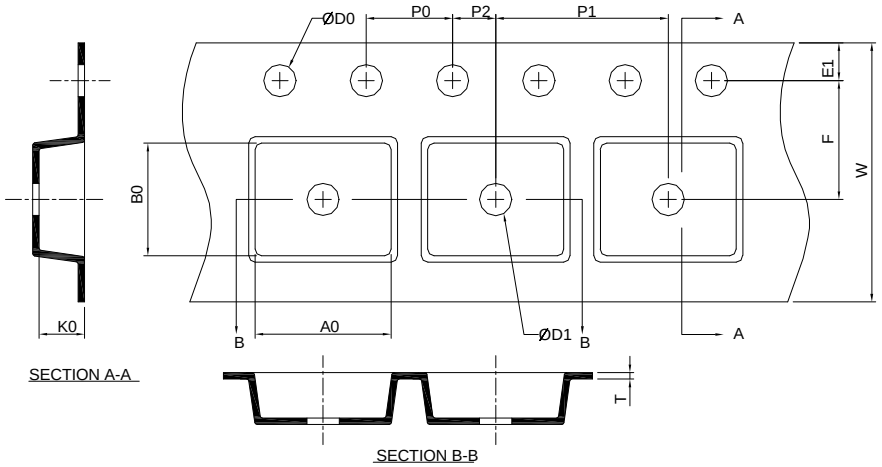


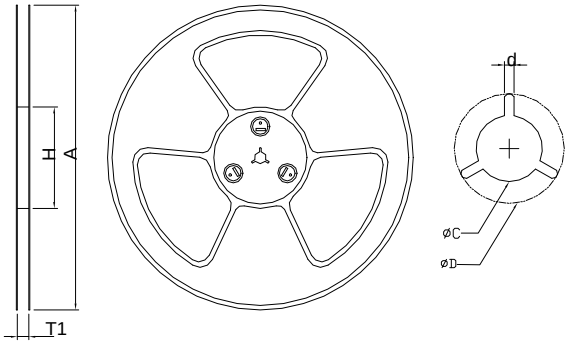
SYMBOL	TQFP7x7-48P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.95	1.05	0.037	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
D	8.80	9.20	0.346	0.362
D1	6.90	7.10	0.272	0.280
D2	3.00	4.50	0.118	0.177
E	8.80	9.20	0.346	0.362
E1	6.90	7.10	0.272	0.280
E2	3.00	4.50	0.118	0.177
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	7°	0°	7°

Note : 1. Followed from JEDEC MS-026 ABC.

2. Dimension "D1" and "E1" do not include mold protrusions. Allowable protrusions is 0.25 mm per side. "D1" and "E1" are maximun plasticbody size dimensions including mold mismatch.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TQFP7x7-48P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	9.4±0.20	9.4±0.20	1.8±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN7x7-48	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	7.30±0.20	7.30±0.20	1.3±0.20

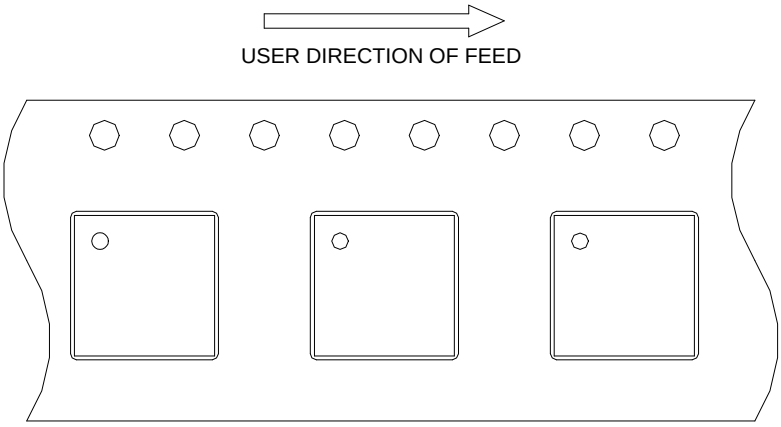
(mm)

Devices Per Unit

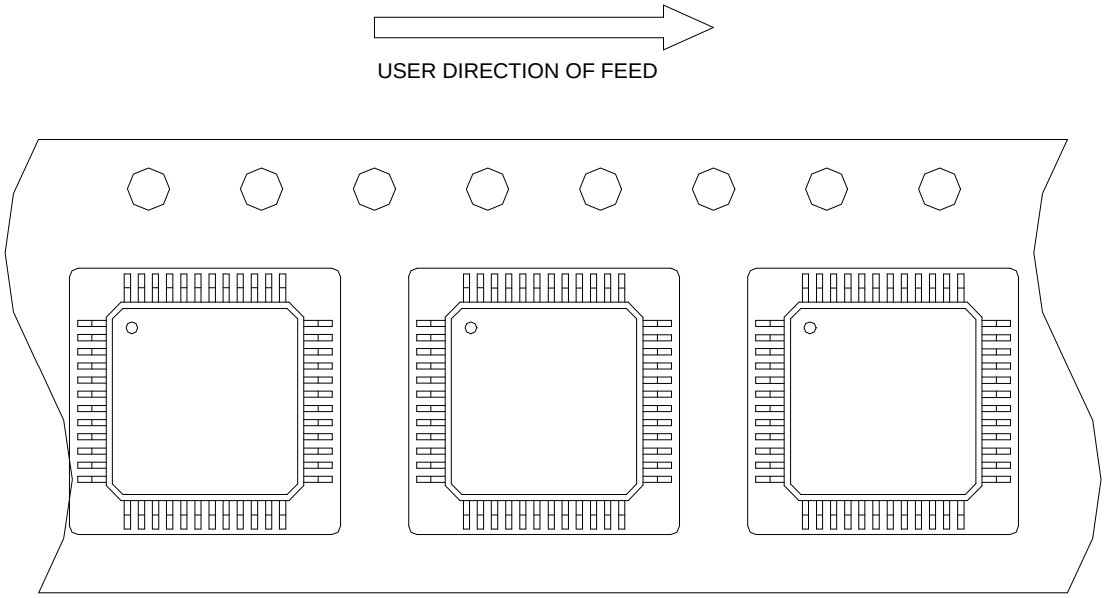
Package Type	Unit	Quantity
TQFP7x7-48P	Tape & Reel	2500
TQFN7x7-48	Tape & Reel	2500

Taping Direction Information

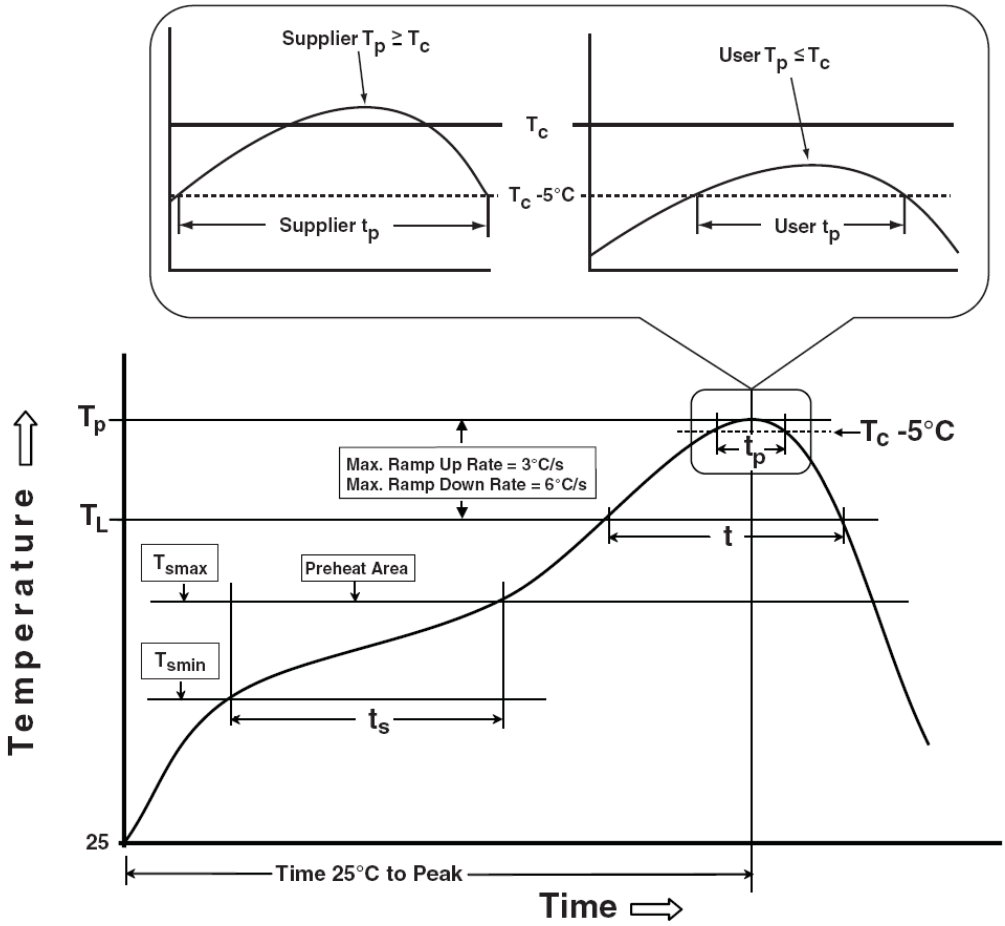
TQFN7x7-48



TQFP7x7-48P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838